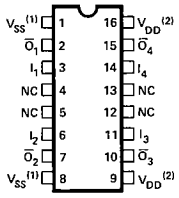
QUAD CCD CLOCK DRIVER

- **Internal Circuitry Minimizes CCD Clock Cross-Coupling Voltage Transients**
- **Drives Four 2416s**
- **Low Standby Power Dissipation: 24mW Typically**
- **TTL Inputs**
- **Single +12V Supply**
- **Standard 16 Pin Dual In-Line Package**

The 5244 is a quad clock driver which provides high capacitive drive suitable for driving charge coupled memories. The 5244 features very low D.C. power dissipation from a single 12V supply with output characteristics directly compatible with the 2416 clock input requirements. Internal circuitry controls the cross-coupled voltage transients between the clock phases generated by the 2416 and limits the transition time so that excessively fast transitions do not occur on the clock line.

The 5244 is fabricated using an advanced ion-implanted, silicon gate, CMOS process.

PIN CONFIGURATION

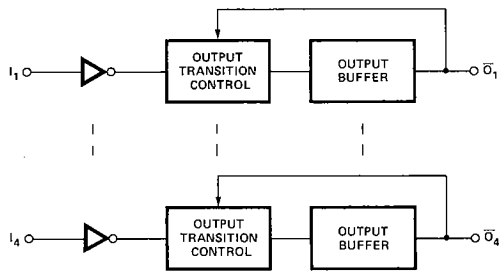


NOTES: 1. BOTH PIN 1 AND 8 MUST BE CONNECTED TO V_{SS}.
2. BOTH PIN 9 AND 16 MUST BE CONNECTED TO V_{DD}.

PIN NAMES

$I_1 - I_4$	TTL INPUT
$\overline{O}_1 - \overline{O}_4$	DRIVER OUTPUT
V_{DD}	+12V POWER SUPPLY
NC	NOT CONNECTED
V_{SS}	GROUND

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to +150°C
Supply Voltage with Respect to V_{SS}	-0.5 to +14V
All Input Voltages	-0.5 to (V_{DD}+1V)
Outputs	-1V to (V_{DD} +1)
Power Dissipation	1.35W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current	-10	±0.1	10	μA	$V_{IN} \leq V_{IL}$
I_{IH}	High Level Input Current	-10	±0.1	10	μA	$V_{IN} \geq V_{IH}$
V_{IL}	Input Low Voltage		+1.2	+0.85	V	
V_{IH}	Input High Voltage	+2.0	+1.5	V_{DD}+1.0	V	
V_{OL}	Output Low Voltage	0	0.03	+0.1	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	V_{DD}-0.1	V_{DD}-.03	V_{DD}	V	I_{OH} = -5mA
I_{DD0}	Standby Current		2.0	4.0	mA	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$, f = 0 MHz
I_{DD1}	Operating Current		75	105[3]	mA	$V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=0.67 MHz[2]

A.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V, Note 2

Symbol	Parameter	Limits Driving 4 2416's Min.	Typ.	Max.	Units
V_{OLT}	Transient Cross-Coupled Output Low Voltage	-0.8	±0.5	+0.8	V
V_{OHT}	Transient Cross-Coupled Output High Voltage	V_{DD}-0.8	V_{DD}±0.5	V_{DD}+0.8	V
t_{PWT}	Transient Cross-Coupled Output Pulse Width			Note 1	ns
Δt_D	Differential Delay of t_{DLH} and t_{DHL} for Drivers in the Same Package			15	ns
t_{DLH1}	Input Low to Output High Delay Time, ϕ_1 or ϕ_3	30	50		ns
t_{DHL1}	Input High to Output Low Delay Time, ϕ_1 or ϕ_3	30	50		ns
t_{TLH1}	Output Rise Time, ϕ_1 or ϕ_3	30	50	75	ns
t_{THL1}	Output Fall Time, ϕ_1 or ϕ_3	30	50	75	ns
t_{PLH1}	Input to Output Delay Plus Rise Time, ϕ_1 or ϕ_3		100	160	ns
t_{PHL1}	Input to Output Delay Plus Fall Time, ϕ_1 or ϕ_3		100	150	ns
t_{DLH2}	Input Low to Output High Delay Time, ϕ_2 or ϕ_4	30	55		ns
t_{DHL2}	Input High to Output Low Delay Time, ϕ_2 or ϕ_4	30	55		ns
t_{TLH2}	Output Rise Time, ϕ_2 or ϕ_4	30	55	85	ns
t_{THL2}	Output Fall Time, ϕ_2 or ϕ_4	30	55	90	ns
t_{PLH2}	Input to Output Delay Plus Rise Time, ϕ_2 or ϕ_4		110	175	ns
t_{PHL2}	Input to Output Delay Plus Fall Time, ϕ_2 or ϕ_4		110	170	ns

Notes: 1. The maximum t_{PWT} is the sum of the output transition time (rise or fall) plus 5ns.

2. Output Load = four 2416 clock inputs or equivalent per Figure 2.

3. $I_{DD1} = 4.0\ mA + \frac{75.4\ mA}{t_{\phi/2}\ (in\ \mu s)}$

CAPACITANCE* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	8	14	pf	f = 1 MHz, V_{bias} = 2V, V_{DD} = 0V

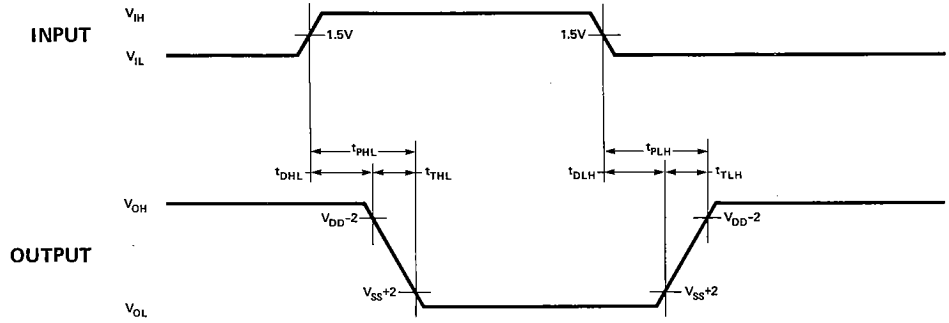
*This parameter is periodically sampled and is not 100% tested.

A.C. Test Conditions

1. TTL Input Levels = 0.4V to 2.4V.
2. Input Rise and Fall Times = 5 ns between 0.9V and 1.9V.
3. Output Load = Four 2416 clock inputs or equivalent per Figure 2.
4. Cross Coupled Voltage Pulse Width measured at ±0.4V and V_{DD} ±0.4V.

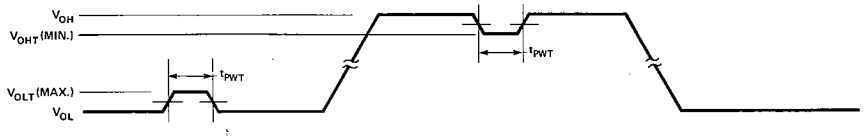
Waveforms

A. INPUT TO OUTPUT DELAY

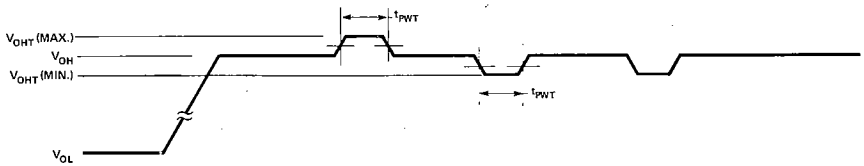


B. 5244 OUTPUT CROSS-COUPLED VOLTAGE (DRIVING FOUR 2416'S)

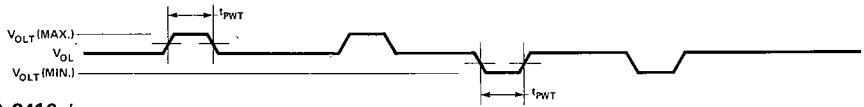
5244 OUTPUT DRIVING 2416 ϕ_1



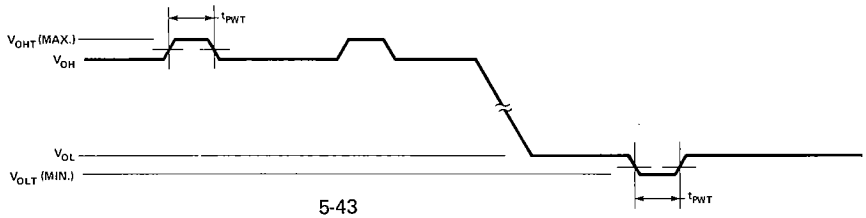
5244 OUTPUT DRIVING 2416 ϕ_2



5244 OUTPUT DRIVING 2416 ϕ_3

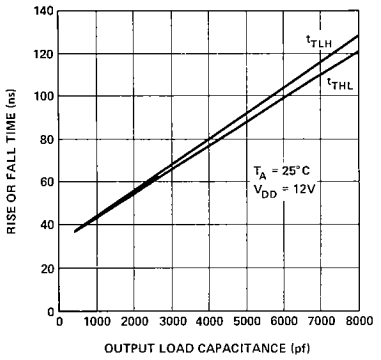


5244 OUTPUT DRIVING 2416 ϕ_4

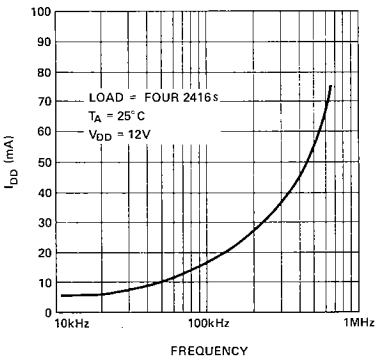


Typical Characteristics

OUTPUT RISE AND FALL TIME VS. CAPACITANCE



I_{DD} VS. FREQUENCY



Application Information

The 5244 is a TTL to MOS level converter designed to drive very high capacitive loads with no required additional external components. Its primary application is to drive the clock phase inputs of the Intel ® 2416, a 16,384 word x 1 bit charge coupled device.

DRIVING THE 2416

The 5244 is designed to drive the clock phase inputs of four 2416s and meet or exceed the electrical specifications of these inputs. The 2416 clock specifications of special interest to the system designs are:

1. Clock transition time.
2. Clock to clock voltage coupling.

Clock Transition Control

The 5244 will meet the min/max clock transition time requirement of the 2416 when driving four 2416s. However, when driving less than four 2416s an external capacitor (C_{ext}) must be added to assure that the minimum clock transition time (30ns) is adhered to. The maximum clock transition time for the 5244 will not be exceeded if C_{ext} is chosen according to the recommendations in Figure 1.

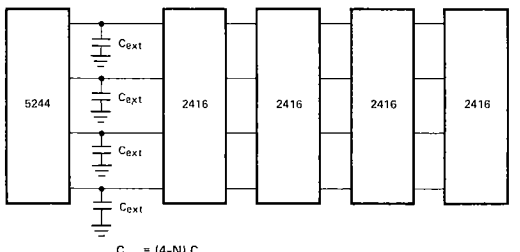


Figure 1. External Loading Requirements When Driving Fewer Than Four 2416s.

Clock Skews

The differential delay of t_{DLH} or t_{DHL} for driver elements in the same package is specified to be Δt_D (15 ns max.). This provides assurance to the system designer that the maximum skew introduced by a 5244 driver package will be limited to Δt_D. As an example, if the fastest t_{DLH} (or t_{DHL}) occurs for I_1 to $\overline{O}_1$ and this is measured to be 45 ns, the output delays for I_2 to $\overline{O}_2$, I_3 to $\overline{O}_3$ or I_4 to $\overline{O}_4$ will be no greater than 60 ns. This should be taken into consideration when designing the TTL source of the four phases required for 2416 operation. To minimize system skew, the four phases associated with any given group of 2416s should be provided from the same 5244 package.

Clock to Clock Voltage Coupling

The equivalent circuit of the 2416 clock phase inputs is shown in Figure 2. The magnitude and duration of the cross-coupling are graphically presented in Waveform B and specified in the A.C. Characteristics. Figure 3, on the next page, shows the noise margin between these specifications and the 2416 input requirements.

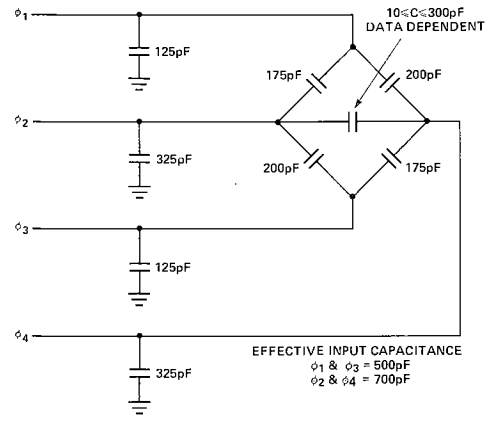


Figure 2. 2416 Equivalent Capacitance Circuit. (Maximum values shown.)

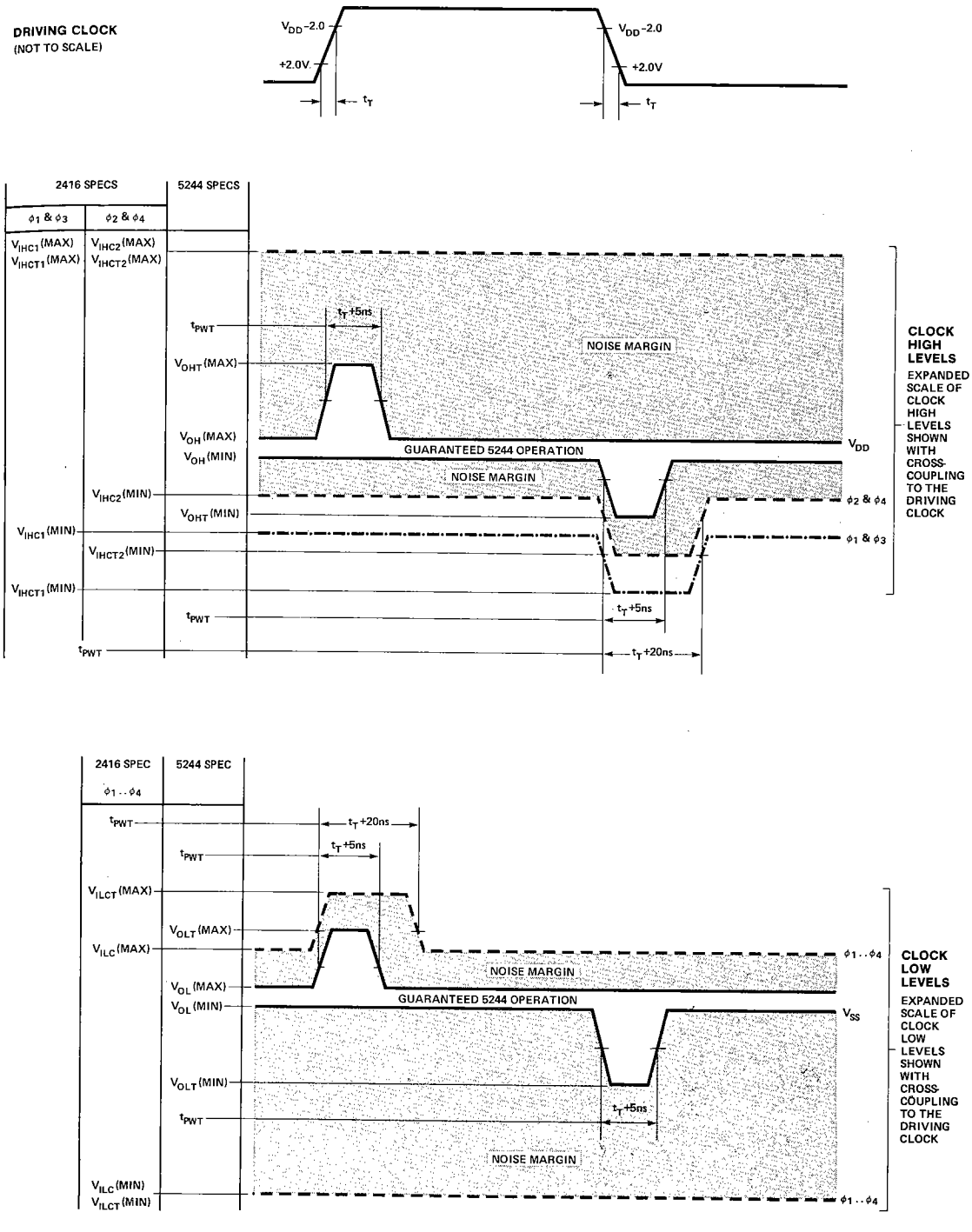


Figure 3. Noise Margins Between 5244 Output Specs and 2416 ϕ_1 . . . ϕ_4 Input Requirements.